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FOR IMMEDIATE RELEASE

Startup Silistix Overcomes "Slow Wire" Communications Problems of Complex SoCs

- ***CHip-Area INterconnect (CHAIN) solution reduces power and simplifies design effort***

San Jose, Calif.- December 19, 2005 – Silistix, a provider of innovative software for on-chip communications solutions, today announced that it is developing EDA tools and libraries to allow designers to more efficiently generate interconnect logic to communicate between intellectual property (IP) blocks in system-on-a-chip (SoC) platforms. The company's CHAIN solution provides power-dissipation and design-productivity improvements over traditional on-chip bus architectures.

The CHAIN interconnect fabric generated by Silistix' design and synthesis tool suite, CHAINworks™, is a self-timed, packet-based interconnect network that manages data flow between IP cores on a chip without being dependent on the edges of a system clock. This results in lower power dissipation since power is dictated by traffic load and not by a fixed clock rate. Clock domains in the CHAIN fabric do not have to be dependent on a system clock and the interconnect fabric can be tuned for specific throughput, area and power targets.

"CHAIN networks represent a new way of looking at on-chip interconnect that eliminates many of the problems associated with traditional global bus architectures controlled by high-speed clocks," said David Fritz, vice president of marketing at Silistix. "Designers can also use Silistix provided adaptors to interface existing synchronous IP blocks to CHAIN networks thereby leveraging existing design work."

Chip design effort is also significantly reduced, especially with respect to timing closure. The problems associated with developing a clock distribution network are eliminated with the CHAIN fabric, as is the need for frequency balancing on the chip.

CHAINworks fits within existing EDA design flows, and the synthesized CHAIN interconnect fabric supports multiple protocols including AHB, APB, and AXI enabling existing IP blocks to be used without modification. The Silistix CHAIN solution targets OEMs, ODMs and fabless semiconductor companies who are developing products for power-sensitive markets such as cellular handsets, portable multimedia devices and smart cards, as well as for companies who are developing SoCs for complex applications such as HDTVs, set-top boxes, network security devices and SAN/NAS (Storage Area Network/Network Attached Storage) devices.

About CHAIN

Systems-on-a-Chip complexity has accelerated to the point that the on-chip interconnection of functional blocks by conventional bus technology cannot meet requirements. Achieving satisfactory communication among multiple clock domains connected by long, slow wires is the most significant SoC design challenge facing designers. Silistix' CHAIN technology provides a solution to the complexity problem in a manner analogous to that used by telephone systems as they migrated from circuit-switched to packet-switched communication, revolutionizing the industry in the process. Similarly, Silistix' solution relegates the 'Timing Closure' issue to a much simpler class of problem, reduces on-chip congestion and overall power consumption. Silistix will announce the features and availability of its CHAINworks™ design-tool suite early in 2006.

About Silistix

Silistix is the leading supplier of on-chip interconnect solutions delivering predictable power, performance and area while cutting overall chip design time and effort. Silistix EDA tools and advanced circuit IP enable design teams to overcome fundamental challenges including global timing closure, clock distribution, power management, and utilization of the latest process technologies while meeting the extreme market pressures of converged consumer electronics products. The company is venture funded and has offices in Manchester, England, San Jose, California, and Tokyo, Japan. For more information on Silistix and its products visit www.silistix.com.

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