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FOR IMMEDIATE RELEASE

Silistix CHAINarchitect Bridges Gap Between Conventional and Leading-Edge Interconnect Methodologies

- *Chip architects can now develop and analyze self-timed SoC interconnect*
- *Ties the chip's architecture to its implementation details*

San Jose, Calif. – May21, 2007 – Silistix, a leading provider of innovative software for the design of on-chip communication solutions, today announced CHAINarchitect, a new tool in the Company's CHAINworks tool suite for developing interconnect networks for SoCs. With CHAINarchitect, chip architects can easily explore new interconnect topologies and perform "what if" analyses to optimize on-chip communications (bandwidth and latency) between IP cores along with overall system characteristics such as power, die area, system-level performance and others.

CHAINarchitect provides a formalized and executable specification methodology for chip architects to develop interconnects that meet system design intent. This allows SoC designers to painlessly make the transition from a time-division multiplexed (TDM), hierarchical bus structure that is running out of steam to a more advanced, on-chip, network-like communications topology using distributed resources. CHAINarchitect helps designers accelerate time to market for their first design and its derivatives.

Designers are 'hitting the wall'

SoC designers are facing serious performance, power, timing closure, complexity, on-chip traffic congestion, and time-to-market challenges. The aggregate demands of multicore architectures, faster clocks and shrinking design nodes limit what can be supported by multiple, hierarchical bus structures. Current on-chip communications, based on global clocks distributed around the chip, are no longer effective and are a limiting factor in achieving maximum system performance. Using self-timed

interconnect saves power, enhances speed, and simplifies design closure, all of which accelerate time to market

“CHAINarchitect is the first tool to provide SoC architects with an executable means of capturing system requirements and automatically creating optimal interconnect solutions.” said David Lautzenheiser, Vice President of Marketing at Silistix.

“CHAINarchitect lets you synthesize flexible, design-specific, self-timed interconnect, with all its time to market, power and performance advantages. Self-timed circuits have emerged from the laboratory and are now ready for production implementation.”

Availability

CHAINarchitect is available immediately on Windows XP Professional and Red Hat Enterprise Linux version 3.6.

About CHAINworks

CHAINworks is a suite of EDA tools for the design and synthesis of customized on-chip interconnect using self-timed (clock-less) circuits. CHAINworks fits into existing chip design flows and reduces design effort, lowers power consumption and simplifies chip layout.

About Silistix

Silistix is the leading supplier of on-chip interconnect solutions delivering predictable power, performance and area while cutting overall chip design time and effort. Silistix EDA tools and advanced circuit IP enable design teams to overcome fundamental challenges including global timing closure, clock distribution, power management, and utilization of the latest process technologies while meeting the extreme market pressures of converged consumer electronics products. The company is venture funded and has offices in Manchester, England, San Jose, California, and Tokyo, Japan. For more information on Silistix and its products visit www.silistix.com.

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