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FOR IMMEDIATE RELEASE

David Fritz Promoted to CEO of Silistix

- *Fritz takes reigns of interconnect company*
- *Company to take a leadership position in SoC design methodology*

San Jose, Calif. – April 7, 2006 – Silistix, a provider of EDA tools for on-chip communications solutions, today announced the promotion of David Fritz from vice president of marketing to Chief Executive Officer (CEO) for the company. As CEO, Fritz will provide Silistix with vision, sales and marketing expertise to generate greater awareness and accelerate customer adoption of its CHAINworks™ suite for the design and synthesis of self-timed interconnect technology for system-on-a-chip (SoC) development.

“We are very pleased to have David accept the position as CEO for Silistix,” said Phil Bishop, chairman of the Silistix board of directors. “As vice president of marketing, David played an integral part in defining the company’s markets and launching the company and its first product. I am confident that David will continue providing the vision and leadership to make Silistix the recognized leader in self-timed on-chip interconnect and an enabler of the next-generation of Semiconductor Devices”

Prior to joining Silistix, Fritz was vice president of marketing and business development for ARC International. He was the founder and president of Production Languages Corporation, a pioneer in configurable processor technology, where he was awarded a U.S. patent covering fundamental processes related to configurable processors. In 1999, ZILOG acquired Production Languages, naming Fritz the vice president of ZiLOG’s Advanced Cores R & D as well as vice president of ZiLOG’s

Development Systems Group. Fritz holds degrees in Mathematics and Computer Science from Manchester College.

About CHAINworks

System-on-a-Chip complexity has accelerated to the point that the on-chip interconnection of functional blocks by conventional bus technology cannot meet design requirements. Achieving satisfactory communication among multiple clock domains connected by long, slow wires is the most significant SoC design challenge facing designers today. Silistix' CHAINworks technology provides a unique and compelling solution to the complexity problem in a manner analogous to that used by telephone systems as they migrated from circuit-switched to packet-switched communication, revolutionizing the industry in the process. Similarly, Silistix' solution relegates the 'Timing Closure' issue to a much simpler class of problem, and reduces on-chip congestion and overall power consumption.

About Silistix

Silistix is the leading supplier of on-chip interconnect solutions delivering predictable power, performance and area while cutting overall chip design time and effort. Silistix EDA tools and advanced circuit IP enable design teams to overcome fundamental challenges including global timing closure, clock distribution, power management, and utilization of the latest process technologies while meeting the extreme market pressures of converged consumer electronics products. The company is venture funded and has offices in Manchester, England, San Jose, California, and Tokyo, Japan. For more information on Silistix and its products visit www.silistix.com.

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