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## **FOR IMMEDIATE RELEASE**

### **Silistix Self-Timed Interconnect Solution Adds Support for AXI Bus Protocol**

- *Extends designer use of popular AMBA buses for asynchronous interconnect on SoCs*

*San Jose, Calif. – July 17, 2006* – Silistix, a provider of innovative software for on-chip communications solutions, today announced that they have added support for the on-chip AMBA™ AXI™ bus protocol with Silistix's synthesized self-timed interconnect technology. The company's CHAIN solution, which already supports the ARM® AMBA AHB™ and APB™ buses, provides power-dissipation and design-productivity improvements over traditional on-chip synchronous bus architectures.

The AMBA 3 AXI (Advanced eXtensible Interface) protocol builds on the many benefits of the AMBA standard by greatly extending the performance and flexibility of AMBA protocol-based systems. The AXI interface enables the easy creation of efficient, high-frequency designs which maximize the use of interconnect resources leading to very high data-throughput. As well as the basic data transfer protocol, the AMBA 3 AXI protocol also includes optional extensions to cover signaling for DMA, interrupts and low-power operation.

The CHAIN interconnect fabric generated by Silistix' design and synthesis tool suite, CHAINworks™, is a self-timed, packet-based interconnect network that manages data flow between IP cores on a chip without being dependent on the edges of a system clock. CHAINworks accelerates design productivity and timing closure while producing chips that have distinct power-dissipation advantages over conventional chips that utilize complex synchronous bus architectures. With the CHAIN interconnect fabric, power is

dictated by traffic load and not by a fixed clock rate. Clock domains in the CHAIN fabric do not have to be derivatives of a system clock, allowing IP blocks to operate at their optimal frequencies. Furthermore, the interconnect fabric can be tuned for specific throughput, area and power targets. Using CHAINworks, designers can synthesize a self-timed CHAIN interconnect that interfaces with synchronous blocks of a SoC, such as processors or peripherals, that are connected through compliant AMBA protocols.

“The ARM-developed AMBA bus protocol continues to be very widely used by SoC designers,” said David Fritz, CEO of Silistix. “By extending support to include the AMBA 3 AXI interface, we are opening up new opportunities for designers to reap the power, performance and design-time advantages of chips that use our self-timed interconnect, particularly in NoC applications.”

“We are seeing accelerated industry adoption of AMBA 3 AXI by designers who want to maximize the speed and functionality of their chips,” adds Brad Suessmith, Director of Marketing, Fabric IP Division, ARM Ltd. “Silistix and ARM share common goals of providing designers with the tools and IP they need to maximize the performance while minimizing the power needed for their leading-edge SoCs.”

CHAINworks fits within existing EDA design flows and generates the interconnect fabric between the various IP blocks. The Silistix solution targets OEMs, ODMs and fabless semiconductor companies who are developing products for power-sensitive markets such as cellular handsets, portable multimedia devices and smart cards, as well as for companies who are developing SoCs for complex applications such as HDTVs, set-top boxes, network security devices and SAN/NAS (Storage Area Network/Network Attached Storage) devices.

### **About CHAIN**

System-on-a-Chip complexity has accelerated to the point that the on-chip interconnection of functional blocks by conventional bus technology cannot meet design requirements. Achieving satisfactory communication among multiple clock domains connected by long, slow wires is the most significant SoC design challenge facing designers. Silistix' CHAIN technology provides a solution to the complexity problem in a manner analogous to that used by telephone systems as they migrated from circuit-switched to packet-switched communication, revolutionizing the industry in the process.

Similarly, Silistix' solution relegates the 'Timing Closure' issue to a much simpler class of problem, and reduces on-chip congestion and overall power consumption.

### **About AXI**

The AMBA 3 AXI (Advanced eXtensible Interface) protocol builds on the many benefits of the AMBA standard by greatly extending the performance and flexibility of AMBA protocol-based systems. With its unidirectional channel architecture, AMBA 3 AXI enables the efficient use of register slices to pipeline the interconnect for higher speed, or to enable the use of multiple clock domains for low power. The support of multiple outstanding transactions and out-of-order transaction completion, together with the efficient use of the read, write and address/control channels enable AMBA 3 AXI protocol-based systems to achieve levels of performance and efficiency limited only by the capabilities of the peripherals themselves.

### **About Silistix**

Silistix is the leading supplier of on-chip interconnect solutions delivering predictable power, performance and area while cutting overall chip design time and effort. Silistix EDA tools and advanced circuit IP enable design teams to overcome fundamental challenges including global timing closure, clock distribution, power management, and utilization of the latest process technologies while meeting the extreme market pressures of converged consumer electronics products. The company is venture funded and has offices in Manchester, England, San Jose, California, and Tokyo, Japan. For more information on Silistix and its products visit [www.silistix.com](http://www.silistix.com).

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