



FOR RELEASE 6 A.M. PDT

June 30, 2009

## Silistix Adds Power Management to their Network-on-Chip

*CHAINpower expands Silistix' Network-on-Chip (NoC) Product Families with Power Management IP*

**SAN JOSE, Calif.,— June 30, 2009** — Silistix Inc. today announced CHAINpower, a new extension to its CHAINworks product line addressing the growing need for integrated clock and power management requirements of modern low-power SoCs.

CHAINpower uses Silistix' industry leading NoC synthesis technology to address the need to intelligently manage the growing number of clock and power domains through the interconnect. Silistix pioneered the use of asynchronous (clockless) networks that provide a natural boundary between chip regions which frequently overlap power domains and isolate clock domains. CHAINpower adds new functionality into the NoC in order to manage the bring-up and shutdown of clock and power domains through a standard management interface by interoperating with protocol specific power intent signaling of OCP and AXI protocols.

“With the smartphone chipset market as the leading indicator, we have seen accelerating demand for tools and technologies that help designers manage the growing number of clock and power domains of their SoCs,” said Silistix Director of Product Marketing David Stratman. “As end-product power budgets shrink, complex SoCs must manage their power domains intelligently and dynamically. The Silistix NoC interconnect, connecting all corners of the chip, provides the most efficient means to do so.”

CHAINpower is an add-on product compatible with any combination of asynchronous, synchronous or mixed asynchronous/synchronous NoCs generated using CHAINworks *Sync* or CHAINworks *GALS*; forming the most consistent and comprehensive methodology for power management on the market today.

### **Availability**

CHAINpower will begin shipping prior to DAC in July 2009.

**About Silistix**

Silistix, Inc. is a leading Silicon Intellectual Property (SIP) vendor, delivering predictable Network-on-Chip (NoC) solutions for managing chip complexity. Silistix CHAIN® works family of tools and IP libraries address timing closure, power management, and deep-sub-micron process variability while cutting chip design time and effort. Silistix is privately held and is backed by a number of venture firms and corporate investors, including Intel Capital. The company has offices in Manchester, England; San Jose, California; and Tokyo, Japan. For more information, visit [www.silistix.com](http://www.silistix.com).

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