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## **FOR IMMEDIATE RELEASE**

### **Silistix Co-Founder John Bainbridge Promoted to CTO**

- *Asynchronous guru to direct company's technology development*

*San Jose, Calif. – March 6, 2006* – Silistix, a provider of innovative software for on-chip communications solutions, today announced the promotion of co-founder and hardware design architect Dr. John Bainbridge to the position of Chief Technical Officer. As CTO, Dr. Bainbridge will provide his expertise and guidance to Silistix as the company expands its product offering to larger markets and continues to develop its CHAIN self-timed interconnect technology for system-on-a-chip (SoC) designs.

“We are very pleased to have John accept the CTO position at Silistix,” said Roy McGuffin, Silistix CEO. “His brilliant work at the University of Manchester, and with the Amulet Program on asynchronous SoC interconnect, helped develop the foundation for Silistix’ CHAIN technology. We are confident that John will be strong visionary force in extending Silistix’ lead in asynchronous interconnect technology.”

Prior to founding Silistix, Dr. Bainbridge was a research fellow in the Department of Computer Science at the University of Manchester, UK. He received a MEng degree in Electronic Systems Engineering in 1996 and his PhD in Computer Science from the University of Manchester in 2001 for work on Asynchronous System-on-Chip Interconnect. Dr. Bainbridge’s pioneering work is the foundation of the company’s interconnect-fabric technology. His thesis, winner of the 2001 British Computer Society/CPHC Distinguished Dissertation Competition, described the design of the MARBLE asynchronous system bus used in the Amulet3i subsystem on the DRACO communications chip.

## **About CHAIN**

System-on-a-Chip complexity has accelerated to the point that the on-chip interconnection of functional blocks by conventional bus technology cannot meet design requirements. Achieving satisfactory communication among multiple clock domains connected by long, slow wires is the most significant SoC design challenge facing designers. Silistix' CHAIN technology provides a solution to the complexity problem in a manner analogous to that used by telephone systems as they migrated from circuit-switched to packet-switched communication, revolutionizing the industry in the process. Similarly, Silistix' solution relegates the 'Timing Closure' issue to a much simpler class of problem, and reduces on-chip congestion and overall power consumption.

## **About Silistix**

Silistix is the leading supplier of on-chip interconnect solutions delivering predictable power, performance and area while cutting overall chip design time and effort. Silistix EDA tools and advanced circuit IP enable design teams to overcome fundamental challenges including global timing closure, clock distribution, power management, and utilization of the latest process technologies while meeting the extreme market pressures of converged consumer electronics products. The company is venture funded and has offices in Manchester, England, San Jose, California, and Tokyo, Japan. For more information on Silistix and its products visit [www.silistix.com](http://www.silistix.com).

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