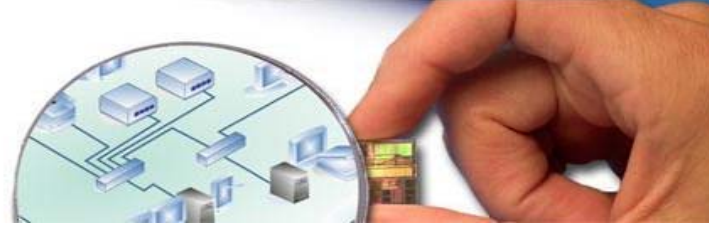


CHAIN[®]works



Overview

The challenge of today's multi-million gate designs is to deal with system-level complexity in the presence of Deep Sub-Micron (DSM) effects on the physical design while coping with extreme development schedule pressures and rapidly escalating development costs. In today's multi-processor systems-on-chip (MPSoCs), subsystems must communicate in parallel, and traditional on-chip buses and crossbars can no longer handle the traffic. Moreover, as design size, clock speeds and process variability issues increase, getting the design implementation to match the design intent (commonly known as design closure) is becoming exceedingly difficult and time-consuming. Current interconnect methods are a big part of that problem and designers are turning to on-chip networks as the solution.

Silistix CHAINworks employs a Network-on-Chip (NoC) approach to achieve predictable interconnect solutions to solve these chip complexity challenges.

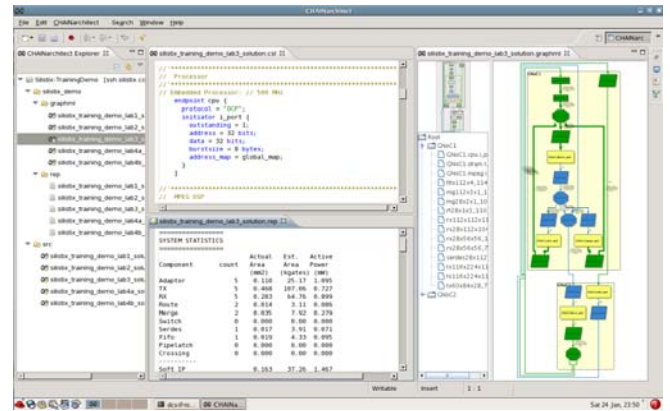
CHAINworks

CHAINworks is Silistix' suite of software tools and libraries of NoC IP components that designers of these complex chips use to design and synthesize NoCs that meet the requirements expressed in a high level description of the system interconnect specification. There are two main variants of the tool suite: **CHAINworks Sync** allows designers to create fully synchronous NoCs implemented purely as synthesizable Verilog RTL code. **CHAINworks GALS** adds Silistix' patented asynchronous NoC technology to allow designers to create **Globally Asynchronous Locally Synchronous** NoCs for highly complex chips in deep submicron processes.

The CHAINworks suite consists of the following tools:

CHAINarchitect

CHAINarchitect is a graphical cockpit used to manage all aspects of architecting, implementing and verifying Silistix NoC solutions. The designer creates, compiles and edits the interconnect requirements, in a format called CSL, and can view performance, power and area (PPA) results and topologies for the generated NoC.

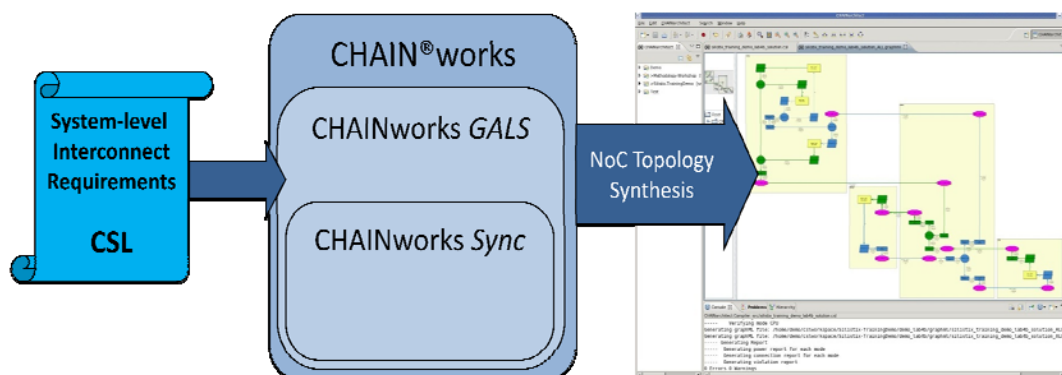


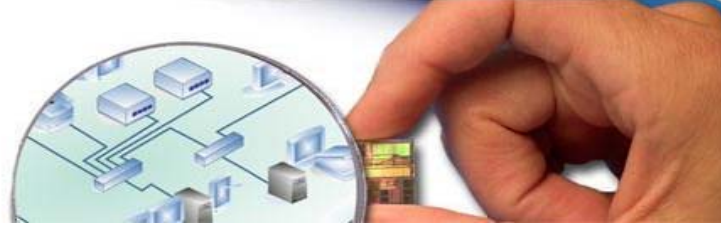
CHAINcompiler

Silistix NoC solutions are synthesized from interconnect requirements, with CHAINcompiler producing the required output logic in various forms including Verilog and SystemC. CHAINcompiler also generates testbenches to facilitate performance validation and verification.

CHAINlibrary

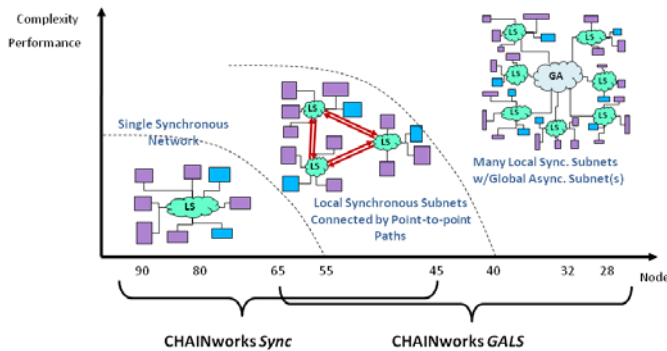
All of the logical building blocks used to construct Silistix NoC solutions are pre-characterized and managed through process specific instances of CHAINlibrary.





CHAINworks Sync

If your next design has multiple bus initiators (aka masters) and you are considering a cross-bar switch based interconnect fabric based for either the AXI or OCP on-chip bus protocols, you would likely benefit from Silistix' entry-level NoC technology. CHAINworks Sync creates fully synchronous NoCs and generates fully synthesizable Verilog RTL code to implement them. The interconnect for more complex, or multi-clock, designs can be implemented as a number of subnets. CHAINworks Sync will automate the connection of these subnets, including the synthesis of synchronizers ("crossings") that can cross different clock domains, whether they are directly or arbitrarily related, or even completed unrelated clocks. All of the tools described previously are included in the CHAINworks Sync suite. All of the interface protocols supported (APB, AHB, AXI, OCP) are available, and design blocks with any of these interfaces can be mixed and matched at will.



CHAINworks GALS

If your next design is highly complex, targeting one of the latest deep submicron processes, has many chip-level connections needing to span the die, has stringent performance and low power requirements, problems with timing closure are expected, or any combination of these factors, then you will likely benefit from CHAINworks GALS. Our flagship suite has all the capabilities of CHAINworks Sync, and additionally lets you synthesize clockless networks and subnets, using Silistix' patented asynchronous circuit technologies. To use CHAINworks GALS, you must have a CHAINlibrary of asynchronous NoC macros specific for your target process and cell library combination. The diagram above shows the kind of designs that would benefit from the GALS approach. Note the overlap for the middle category of designs. A purely synchronous approach will have the lowest gate area (but not necessarily the lowest wire area). The GALS approach will increase gate area, but reduce dynamic power, eliminate global clock skew and

timing closure issues (these will only exist at the synchronous subnet level), improve signal integrity (SI) and reduce susceptibility to process variability.

Note that using a number of synchronous subnets with point-to-point connections using synchronizers to cross clock domains, is described by some as a GALS approach. Silistix can achieve this kind of NoC topology with CHAINworks Sync. In contrast, CHAINworks GALS implements NoC topologies using truly clockless paths and networks using asynchronous NoC components, for the Global Asynchronous subnets. We refer to this as a "true GALS" approach. Silistix' ability to implement a true GALS NoC implementation for the most complex designs in the latest process technologies, as shown at the top-right of the diagram, is unique in the industry.

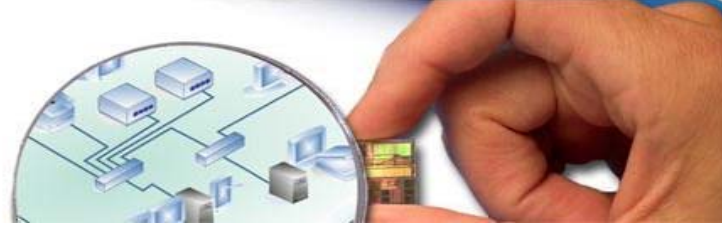
CHAINworks Capabilities:

- ❖ **Requirements capture** at a higher level of abstraction and NoC synthesized from requirements
- ❖ **Architecture optimization** through quick in-tool iterations and simulation at various abstraction levels
- ❖ **Routing congestion** reduced by utilizing narrow links
- ❖ **Multiple bus protocols** supported and translated between – currently APB, AHB, AXI and OCP
- ❖ **Multiple clock & power domains** configurable through tool enabling subsystem reuse in platforms
- ❖ **Packetization, Interleaving, & Serialization** to reduce traffic congestion and maximize use of on-chip resources
- ❖ **Variable link widths** optimized for the aggregate specified traffic flow
- ❖ **Automated testbench generation** for performance validation and verification of synthesized NoC, plus simulation model generation in Verilog and/or SystemC

CHAINworks GALS-only Capabilities:

- ❖ **Reduced power** in asynchronous links – power is only consumed when data is moved
- ❖ **Immunity to process variability** since the asynchronous circuits always work despite Vt variations and switching speeds
- ❖ **Clock trees balancing** simplified by eliminating skew requirements between system components
- ❖ **Global timing closure** eliminated by using truly asynchronous links between subsystems

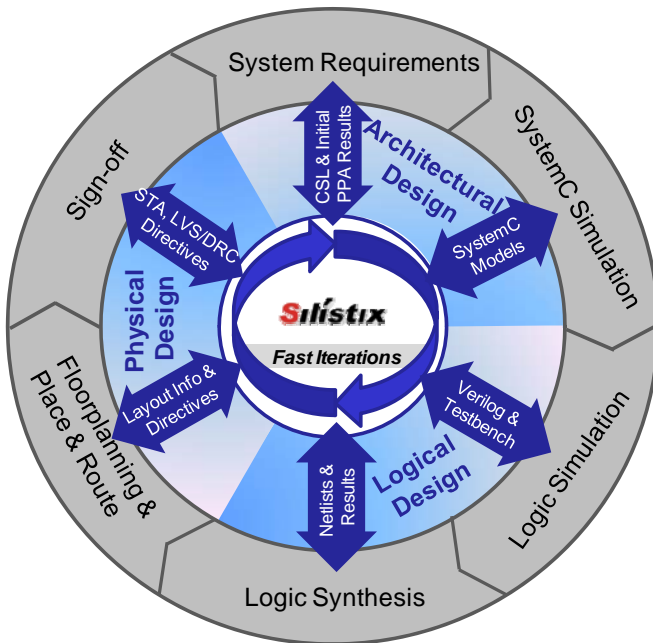
Benefits Summary



CHAINworks Capability	Benefit to Designer
Tool generates optimal NoC topology from high-level interconnect requirements	Reduced design effort, lowers Engineering costs
True GALS NoC technology eliminates global timing closure issues	Reduced schedule risk, shortens TTM (Time To Market)
Supports all common on-chip bus protocol standards, which can be mixed-ad-hoc	Easier design reuse for quick derivative designs, lower NRE
Tool provisions network to carry all specified traffic simultaneously	Predictable performance, power and area
Network topologies scale to optimize area for any size device	Reduced device cost
NoC technology supports today's power management techniques – multiple clock domains, DVFS, shut-down...	Reduced power consumption, lower unit cost

Design Flow Integration

Silistix CHAIN®works provides for rapid iterations on critical decision points in the three key design steps for complex chips: Architectural Design, Logical Design and Physical Design. Standard file formats and script languages are used to provide tight integration between CHAINworks and commonly used EDA tools for each of these design steps.



ESL: CoWare, OSCI/IEEE-compliant SystemC

Simulation: Cadence, Mentor, Synopsys

Synthesis: Cadence, Magma, Synopsys

Physical/Back-end: Cadence, Magma, Mentor, Synopsys

CHAINworks' ability to speed the architectural, logical and physical design convergence, derived from the system-level connection requirements and enabled by tight integration with standard EDA tools in all three steps, is what Silistix terms Interconnect-Driven Design.

Supported Platforms

Linux (Red Hat Enterprise Linux 3,4,5)

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