



Media Contacts:

Silistix
Tom Katherman
Tel: 408-833-9311
Email: tek@silistix.com

Cain Communications (for Silistix)
Jim Lipman
Tel: 925-606-1370
Email: jlipman@caincom.com

**Silistix and CoWare Developing ESL-Based Design Flow for Chips
Using Asynchronous Self-Timed Interconnect**

- *Silistix to demonstrate ESL design for chips using self-timed interconnect at Design Automation Conference*

San Jose, Calif. – July 20, 2006 – Silistix, a provider of innovative software for on-chip communications solutions, today announced that they are developing solutions for SystemC electronic system level (ESL) SoC development using Silistix’s CHAIN self-timed interconnect fabric. The company will integrate Silistix’s CHAINworks™ tool suite with CoWare Platform Architect and CoWare Model Designer to allow designers to assemble and simulate an SoC platform incorporating processors and peripherals from the CoWare Model Library, connected with Silistix’s CHAIN fabric.

CoWare enables platform-driven ESL design by providing a standards-based modeling, simulation, and debug environment for capturing complex IP blocks and verifying them at the transaction-level in SystemC. The CoWare tools speed up the concurrent design of SoCs with embedded software, enabling designers to rapidly create and validate SoC designs at the transaction level in SystemC, thus enabling “what-if” analyses of different chip architectures and choosing the one that best meets specific system requirements.

The CoWare Model Library provides designers with high-quality, high-performance SystemC IP models such as embedded processors, peripherals and memory.

“Partnering with CoWare broadens the opportunities for designers to implement chips that use our clock-less interconnect,” stated David Fritz, Silistix CEO. “The increasing complexity of SoCs is pushing the design community to incorporate ESL tools into the design flow, allowing them to identify and resolve system problems earlier in the design cycle. Working with a leader like CoWare allows our common customers take advantage of a superior set of ESL design tools while reaping the benefits of self-timed interconnect in their chips.”

"We are very pleased to combine our ESL design tools and expertise with Silistix's self-timed interconnect development tools," said A.K. Kalekos, vice president of marketing and business development at CoWare. "The resulting solution will provide SoC designers with distinct design and power advantages, allowing them to get their products to market faster and with better performance."

Silistix to demonstrate ESL chip design with self-timed interconnect at DAC

Silistix will be demonstrating the results of the collaborative effort between Silistix and CoWare in Silistix's Booth (#1714) at this summer's Design Automation Conference (DAC) in San Francisco, CA, July 24-27. The demonstration will show CHAINworks integrated with the CoWare Platform Architect and CoWare Model Designer ESL tools.

About CHAINworks

Silistix's CHAINworks tool suite generates the interconnect fabric between the various IP blocks. CHAINworks takes a description of the initiator and target ports of an SoC design and synthesizes a structural netlist for an interconnect system. CHAINdesigner™, a design exploration tool, takes a description of the connectivity and ports of a design and generates the structure of the fabric along with link widths and fine-grained pipeline stages to balance area, speed and power tradeoffs. CHAINcompiler™ takes the constrained netlist generated by CHAINdesigner and components from CHAINlibrary™, an asynchronous interconnect component library, to produce the structural netlist suitable for inclusion into the targeted SoC. This netlist is then input into to a logic-synthesis tool and mapped to standard cells. Chips using CHAIN self-timed interconnect provide significant power and design advantages over chips that are data-rate limited by a global system clock.

About Silistix

Silistix is a venture-funded spin-out of the University of Manchester, UK, with backing from Intel Capital. The company's focus is on the development and deployment of EDA tools for the design and synthesis of self-timed CHAIN technology for complex system-on-a-chip (SoC) communication. The company has offices in Manchester, England, San Jose, California, and Tokyo, Japan. For more information call 408-573-6104 or visit www.silistix.com.

About CoWare

CoWare is the leading supplier of system-level electronic design automation (EDA) software tools and services. CoWare offers a comprehensive set of electronic system-level (ESL) tools that enable SoC developers to "differentiate by design" through the creation of system-IP including embedded processors, on-chip buses, and DSP algorithms; the architecture of optimized SoC platforms; hardware/software co-design; and virtual platforms for device software development. The company's solutions are based on open industry standards including SystemC. CoWare's customers are major systems, semiconductor, and IP companies in the market where consumer electronics, computing, and communications converge. CoWare's corporate investors include ARM [(LSE:ARM);(Nasdaq:ARMHY)], Cadence Design Systems (NYSE:CDN), STMicroelectronics (NYSE:STM), and Sony Corporation (NYSE:SNE). CoWare is headquartered in San Jose, Calif., and has offices around the world. For more information about CoWare and its products and services, visit <http://www.coware.com>.

###