

## Portable Multimedia Test Chip



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### **Silistix Partners with Tensilica to Develop a Demonstration Test Chip for Portable Multimedia Applications**

- *Companies team with Denali and sci-worx to prove effectiveness of self-timed interconnect technology for multimedia*
- *Test chip to be developed for 65nm process*

**San Jose, Calif. – June 26, 2006** – Silistix, a provider of innovative software for on-chip communications solutions, and Tensilica, a developer of configurable and standard microprocessor cores, announced that they are collaborating on a demonstration chip for low-power, portable multimedia applications. The CMOS chip will demonstrate the ability of the Silistix CHAIN self-timed interconnect technology to work with high-performance processor cores from Tensilica along with additional silicon cores from Denali and sci-worx at a 65nm process node.

“We are extremely pleased to work with such excellent partners for developing a proof-of-concept for the world’s first self-timed A/V player,” said David Fritz, CEO at Silistix. “Choosing a complex A/V design that will be implemented in the leading-edge CMOS process will demonstrate the viability and scalability of self-timed interconnect for performance- and power-critical SoC designs.”

“Multimedia is being added to new consumer devices at an incredible rate, and our customers need an easy-to-integrate, silicon-proven audio and video solution,” said Chris Rowen, Founder, President and Chief Executive Officer of Tensilica. “This test chip

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design will demonstrate to our mutual customers the advantages of using the Silistix interconnect in complex multi-core designs.”

The portable multimedia chip will duplicate much of the functionality of an existing audio/video (A/V) evaluation board, the sci-worx sci-Board-Mobile III, used for the development, test and validation of high-performance multimedia applications. Silistix, Tensilica and their partners are developing the demonstration chip to show the interoperability, low power, and high performance that can be achieved in a typical SoC at a leading-edge process node using a self-timed interconnect system. One of the benefits of Silistix’s self-timed networks is the ability to quickly create a design using existing Silicon IP cores and quickly achieve timing closure for that design.

The demonstration chip will comprise approximately 800K gates of logic and 96kBytes of SRAM. The chip combines the IP of four companies: Denali, Silistix, sci-worx and Tensilica.

#### ***Denali Memory Controller Core***

Denali provides a complete infrastructure for configuring, analyzing, and generating the optimal memory controller for a given customer application. In this case, Denali’s Databahn™ memory controller IP was configured for optimal video data throughput between the Mobile DDR devices and processing units. To ensure low power operation, the controller was also configured to utilize the advanced low-power modes unique to the Micron DDR devices. Denali also provided a DDR physical interface (PHY), specially suited for low power applications, which offers excellent read/write margins while minimizing power consumption.

#### ***Silistix Self-Timed Interconnect***

Silistix’ contribution includes the company’s asynchronous interconnect fabric for connecting the various cores and controller functions of the test chip. Silistix will also contribute an asynchronous traffic instrumentation block to the test chip for evaluating the chip’s performance.

Silistix’s CHAINworks™ tool suite generates the interconnect fabric between the various IP blocks. CHAINworks takes a description of the initiator and target ports of an SoC design and synthesizes a structural netlist for an interconnect system. CHAINdesigner™, a design exploration tool, takes a description of the connectivity and ports of a design and generates the structure of the fabric along with link widths and fine-grained pipeline stages to balance area, speed and power tradeoffs. CHAINcompiler™ takes the constrained netlist generated by CHAINdesigner and components from CHAINlibrary, an asynchronous interconnect component library, to produce the structural netlist suitable for inclusion into the targeted SoC. This netlist is then input into to a conventional logic synthesis tool and mapped to standard cells.

#### ***Sci-Worx Core***

Video decoding on the demonstration multimedia chip is done by sci-worx’s MuViStar 4000, a software programmable multi-standard video decoder and encoder core based on

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an optimized Tensilica Xtensa processor. MuViStar is fully programmable to support all popular video codecs and resolutions up to D1 (decoding). The multimedia chip also uses a second sci-worx core, an LCD interface for controlling an external 640 x 480 LCD display.

#### *Tensilica Cores*

The demonstration chip uses two additional Tensilica Diamond Standard series cores in addition to the video-core. The Diamond Standard 232L CPU is the system controller, running the Linux operating system. The 232L core is a low-power, high-performance, fully synthesizable 32-bit RISC SOC controller core with an MMU (memory management unit) for Linux. The Diamond Standard 330HiFi core is processing audio for this multimedia chip. Most popular audio codecs have been pre-ported to the Diamond 330HiFi core, which makes it a “drop-in” block for any SOC application requiring 24-bit audio capabilities. Specialized audio instructions designed into the Diamond 330HiFi improve code density (reducing memory and power) and reduce speed requirements (lowering power). Techniques used to define these custom instructions include Single Instruction, Multiple Data (SIMD - parallelization), VLIW (multiple operations per cycle), and flexible data path widths (optimum data widths to reduce power).

#### **About Silistix**

Silistix is a venture-funded spin-out of the University of Manchester, UK. The company's focus is on the development and deployment of EDA tools for the design and synthesis of self-timed interconnect technology for complex system-on-a-chip (SoC) communication. The company has offices in Manchester, England, San Jose, California, and Tokyo, Japan. For more information call 408-573-6104 or visit [www.silistix.com](http://www.silistix.com).

#### **About Tensilica**

Tensilica offers the broadest line of controller, CPU and specialty DSP processors on the market today, in both an off-the-shelf format via the Diamond Standard Series cores and with full designer configurability with the Xtensa processor family. Tensilica's low-power, benchmark proven processors have been designed into high-volume products at industry leaders in the digital consumer, networking and telecommunications markets. All Tensilica processor cores are complete with a matching software development tool environment, portfolio of system simulation models, and hardware implementation tool support. For more information on Tensilica's patented approach to the creation of application-specific building blocks for SOC design, visit [www.tensilica.com](http://www.tensilica.com).

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