



Media Contacts:

Silistix
David Fritz
Tel: 408-573-6104
Email: david.fritz@silistix.com

Cain Communications
Jim Lipman
Tel: 925-606-1370
Email: jlipman@caincom.com

Silistix Announces CHAINworks™ for Self-Timed Interconnect Design and Synthesis for SoCs

- *Tool suite works with conventional chip design flows*
- *Accelerates SoC design time and lowers power dissipation*
- *First third-party interconnect with EDA business model*

San Jose, Calif. – January 16, 2006 – Silistix, a provider of innovative software for on-chip communications solutions, today announced CHAINworks™, a suite of tools for development of self-timed interconnect, called CHAIN fabrics, on a system-on-a-chip (SoC). CHAINworks accelerates design productivity and produces chips that have distinct power dissipation advantages over conventional chips that utilize clock-enabled dataflow with traditional buses.

“With CHAINworks, SoC designers can implement self-timed CHAIN interconnect fabrics that provide significant power and design advantages over chips that are data-rate limited by a global system clock,” said David Fritz, vice president of marketing at Silistix. “To accelerate the adoption of our technology we have developed design tools that let designers combine our self-timed CHAIN fabric with conventional synchronous IP cores on the same chip.”

The CHAINworks tool suite takes a description of the initiator and target ports of an SoC design and synthesizes a structural netlist for a CHAIN interconnect. The suite comprises three tools: CHAINdesigner™ for design exploration, CHAINcompiler™ for CHAIN fabric synthesis, and CHAINlibrary™, which is an interconnect component library.

A chip designer uses CHAINdesigner to take a description of the connectivity and ports of a design and generates the structure of the CHAIN fabric along with link widths and fine-grained pipeline stages to balance area, speed and power tradeoffs. With

CHAINdesigner's graphical user interface, the designer can place network gateways, connect ports to clients, and either manually or automatically create a CHAIN topology. CHAINdesigner generates a Verilog or SystemC description of the fabric for simulation, simulation testbenches, constrained CHAIN netlists for input to CHAINcompiler.

CHAINcompiler takes the constrained CHAIN netlist generated by CHAINdesigner and components from CHAINlibrary to produce the structural netlist suitable for inclusion into the targeted SoC. The structural netlist is then input into to a conventional logic synthesis tool such as Synopsys' Design Compiler and mapped to standard cells. CHAINcompiler also creates scripts for static-timing analysis (STA), and hints for downstream place and route (P&R) operations.

"As SoCs include an increasing number of highly complex IP cores, the task of connecting these cores together is becoming overwhelming," said Jerry Worchel, Principal Analyst with high tech market research firm InStat. "With CHAINworks, Silistix appears to have found a way to implement asynchronous self-timed connectivity onto a chip within an existing design flow, minimizing or even eliminating many of the problems associated with traditional synchronous bus structures."

CHAINworks fits within existing EDA design flows and targets OEMs, ODMs and fabless semiconductor companies developing products for power-sensitive markets such as cellular handsets, portable multimedia devices and smartcards, as well as for companies who are developing SoCs for complex applications such as HDTVs, set-top boxes, network security devices and SAN/NAS (Storage Area Network/Network Attached Storage) devices.

Business Model

Silistix' CHAINworks is the first third-party interconnect product to take advantage of the widely accepted EDA business model rather than an IP model, thereby improving per-chip margins by shifting cost from COGS to development.

About CHAIN

System-on-a-Chip complexity has accelerated to the point that the on-chip interconnection of functional blocks by conventional bus technology cannot meet design requirements. Achieving satisfactory communication among multiple clock domains connected by long, slow wires is the most significant SoC design challenge facing designers. Silistix' CHAIN technology provides a solution to the complexity problem in a manner analogous to that used by telephone systems as they migrated from circuit-switched to packet-switched communication, revolutionizing the industry in the process. Similarly, Silistix' solution relegates the 'Timing Closure' issue to a much simpler class of problem, and reduces on-chip congestion and overall power consumption.

Product Availability and Pricing

The first production release of CHAINworks will be available early second quarter, 2006 and will be priced similarly to Synopsys' Design Compiler.

About Silistix

Silistix is a venture-funded spin-out of the University of Manchester, UK. The company's focus is on the development and deployment of EDA tools for the design and synthesis of self-timed interconnect technology for complex system-on-a-chip (SoC) communication. The company has offices in Manchester, England, San Jose, California, and Tokyo, Japan. For more information call 408-573-6104 or visit www.silistix.com.

###